AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, ~~each processor coupled to the integrated switch through~~ wherein a Host Channel Adapter (HCA) couples the first processors to the first switch.

3. (Currently Amended) The node of Claim 2, ~~each processor further coupled to the integrated switch through~~ wherein a peripheral component interconnect (PCI) bridge further couples the first processors to the first switch.

4. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, ~~at least two of the processors communicably coupled directly to each other via~~ wherein a link supporting processor-to-processor communication communicably couples the first processors directly to each other.

5. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, ~~each processor communicably coupled to the integrated switch through~~ wherein a Northbridge communicably couples the first processors to the first switch.

6. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, wherein the ~~integrated~~ first switch is operable to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

7. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, wherein the integrated switch ~~comprising~~ comprises twenty-four ports and ~~enabling~~ enables a toroidal topology comprising four dimensions.

8. (Currently Amended) The node of ~~Claim 1,~~ Claim 28, wherein the integrated switch is operable ~~to:~~ to communicate a first message from a first one of the first processors and a second message from a second one of the first processors in parallel.

~~communicate a first message from a first of the two or more processors; and~~

~~communicate a second message from a second of the two or more processors, the first and second message communicated in parallel.~~

9. (Currently Amended) A system comprising a plurality of interconnected nodes, each node comprising:

a first motherboard;

~~a switch comprising eight or more ports, the switch integrated on the motherboard and operable to interconnect at least a subset of the plurality of nodes; and~~

~~at least two processors, each processor communicably coupled to the integrated switch and integrated on the motherboard.~~

at least two first processors integrated onto the first motherboard and operable to communicate with each other via a direct link between them; and

a first switch integrated onto the first motherboard, the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to at least six second motherboards that each comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard operable to communicably couple the second processors to the first motherboard and at least five third motherboards that each comprise at least two third processors integrated onto the third motherboard and a third switch integrated onto the third motherboard;

the first processors operable to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard;

the first processors operable to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

10. (Currently Amended) The system of Claim 9, ~~the two or more processors on each node coupled to the integrated switch through~~ wherein a Host Channel Adapter (HCA) couples the first processors to the first switch.

11. (Currently Amended) The system of Claim 10, ~~the two or more processors on each node further coupled to the integrated switch through~~ wherein a peripheral component interconnect (PCI) bridge further couples the first processors to the first switch.

12. (Currently Amended) The system of Claim 9, wherein, ~~on~~ at each of one or more of the nodes, ~~at least two of the processors on the node are communicably coupled directly to each other via~~ a link supporting processor-to-processor communication communicably couples the first processors directly to each other.

13. (Currently Amended) The system of Claim 9, ~~the two or more processors on each node communicably coupled to the integrated switch through~~ wherein a Northbridge communicably couples the first processors to the first switch.

14. (Currently Amended) The system of Claim 9, wherein the ~~integrated switch of each node~~ first switch is operable to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

15. (Currently Amended) The system of Claim 9, ~~the integrated switch of each node comprising~~ wherein the first switch comprises twenty-four ports and ~~enabling~~ enables a toroidal topology comprising four dimensions.

16. (Currently Amended) The system of Claim 9, wherein the plurality of nodes are arranged in a ~~topology, the~~ topology enabled by the ~~integrated fabric~~ first switch of each of the plurality of nodes. ~~node.~~

17. (Currently Amended) The system of Claim 16, wherein the topology ~~comprising~~ comprises a hypercube.

18. (Currently Amended) The system of Claim 16, wherein the topology ~~comprising~~ comprises a folded topology.

19. (Currently Amended) The system of Claim 9, wherein a first node of the plurality of nodes is interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis that is perpendicular to the X axis, a fourth node of the plurality of nodes along a Z axis that is perpendicular to the X and Y axes, and a fifth node along a diagonal axis that is oblique to one or more of the X, Y, or Z axes.

20. (Currently Amended) The system of Claim 19, wherein the connection between the first node and the fifth node is operable to reduce message jumps among the plurality of nodes.

21. (Currently Amended) A method comprising:

~~integrating a switch with a motherboard, the integrated switch comprising eight or more ports;~~

~~integrating at least two processors with the motherboard; and~~

~~coupling each processor with the integrated switch.~~

integrating at least two first processors onto a first motherboard, the first processors being operable to communicate with each other via a direct link between them; and

integrating a first switch onto the first motherboard and coupling the first switch to the first processors, the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to at least six second motherboards that each comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard operable to communicably couple the second processors to the first motherboard and at least five third motherboards that each comprise at least two third processors integrated onto the third motherboard and a third switch integrated onto the third motherboard, the first processors operable to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard, the first processors operable to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

22. (Currently Amended) The method of Claim 21, wherein ~~coupling each processor with the integrated switch~~ coupling the first switch to the first processors comprises coupling each one of the first processors to the ~~integrated~~ first switch through a Host Channel Adapter (HCA).

23. (Currently Amended) The method of Claim 22, wherein ~~coupling each processor with the integrated switch~~ coupling the first switch to the first processors comprises coupling each one of the first processors to the ~~integrated~~ first switch through a peripheral component interconnect (PCI) bridge.

24. (Currently Amended) The method of Claim 21, further comprising coupling at least two of the first processors directly to each other via a link supporting processor-to-processor communication.

25. (Currently Amended) The method of Claim 21, wherein coupling ~~each~~ the first processors ~~with~~ to the ~~integrated~~ first switch comprises coupling each one of the first processors ~~communicably~~ to the ~~integrated~~ first switch through a Northbridge.

26. (Currently Amended) The method of Claim 21, wherein the ~~integrated~~ first switch is operable to communicate input/output (I/O) messages at a bandwidth that is approximately equal to a processing speed of the first processors.

27. (Currently Amended) The method of Claim 21, wherein the integrated switch ~~comprising~~ comprises twenty-four ports and ~~enabling~~ enables a toroidal topology comprising four dimensions.

28. (Currently Amended) A node comprising:

a first motherboard;

at least two first processors integrated onto the first motherboard and operable to communicate with each other via a direct link between them; and

a first switch integrated onto the first motherboard, the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to at least six second motherboards that each ~~comprising~~ comprise at least two second processors integrated onto the second motherboard and a second switch integrated onto the second motherboard operable to communicably couple the second processors to the first motherboard and at least five third motherboards that each ~~comprising~~ comprise at least two third processors integrated onto the third ~~motherboards~~ motherboard and a third switch integrated onto the third motherboard ~~motherboards, the first processors operable to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard~~;

the first processors ~~being~~ operable to communicate with particular second processors on a particular second motherboard via the first switch and the second switch on the particular second motherboard;

the first processors ~~being~~ operable to communicate with particular third processors on a particular third motherboard via the first switch, a particular second switch on a particular second motherboard between the first motherboard and the particular third motherboard, and the third switch on the particular third motherboard without communicating via either second processor on the particular second motherboard.

29. (Previously Presented) The node of Claim 28, further comprising an input port and an output port.

30. (Currently Amended) The node of Claim 5, comprising at least two Northbridges, each Northbridge communicably coupling one of the ~~at least two~~ first processors to the ~~integrated~~ first switch.

31. (Currently Amended) The system of Claim 13, each node comprising at least two Northbridges, each Northbridge communicably coupling one of the ~~at least two~~ first processors ~~on the node~~ to the first switch ~~on the node~~.

32. (Currently Amended) The method of Claim 25, wherein the motherboard comprises at least two Northbridges, each Northbridge communicably coupling one of the ~~at least two~~ first processors ~~with~~ to the ~~integrated~~ first switch.

33. (Currently Amended) The system of Claim 9, wherein a first node of the plurality of nodes is interconnected to a second node, a third node, a fourth node, and a fifth node, the first node being the same as the second, third, fourth, and fifth nodes, the first node being operable to communicate with each of the second, third, fourth, and fifth nodes via the interconnections.